DIGITAL AND ANALOG FREQUENCY - TEMPERATURE COMPENSATION OF DIELECTRIC RESONATOR OSCILLATORS

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SUMMARY

The advent of the varactor tuned, dielectric resonator oscillator (DRO) has made possible both digital and analog frequency - temperature compensation (1). Both techniques provide the DRO with a stability approximating that of a crystal referenced oscillator (i.e., better than ±50 ppm over -55^{o} to $+85^{o}C$) without the higher power consumption and spurious output signals.

INTRODUCTION

Microwave oscillators phase-locked to low frequency crystal referenced oscillators have long been used as high stability signal sources. These devices often produce undesirable spurious signals and suffer from "out-of-lock" conditions. In addition, these sources require high input power, large size and high cost. The dielectric resonator oscillator can offer stability comparable to a crystal referenced oscillator over a very limited temperature range. This paper describes both digital and analog compensation techniques which enable the DRO to achieve a frequency - temperature stability comparable to that of a crystal referenced oscillator over a wide temperature range.

DIGITAL COMPENSATION

A functional diagram of the digital frequency - temperature compensation circuit is shown in Figure 1. The temperature sensor is mounted near the active device of the oscillator in order to accurately detect temperature changes. This temperature data is digitized and characterized into 2^{Nth} break points, where N is the number of bits used for conversion(2). An EPROM is programmed with a customized look-up table which provides corrections directly to each digitized temperature word. Each new digital word is latched into a D/A converter by using a delay timer. Digital synchronization is then achieved between the A/D and D/A converters. The analog output voltage is applied to the tuning varactor of the DRO to correct the frequency drift with temperature.

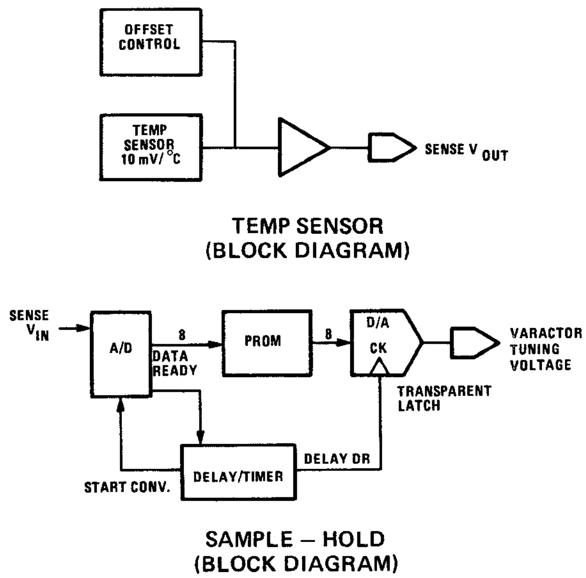

FIGURE 1.

Automatic measurement of the DRO's frequency vs temperature characteristic, calculation of the correction required and programming of the EPROM is accomplished by the system shown in Figure 2. The digital compensation sequence begins with the operator assigning a fixed desired frequency. The controller adjusts the temperature of the platform and allows the oscillator to reach temperature equilibrium before measuring the one-LSB modulation sensitivity. The program then proceeds to calculate the frequency error and determines a new data word. The controller then repeats this frequency measurement loop until the error is less than or equal to one-half the one-LSB modulation sensitivity value. This process continues with a new data word stored at each temperature address until the final temperature is reached. A linear approximation is used in determining the data value between two temperature address steps. The last program routine transfers data words to the PROM programmer and instructs it to program the EPROM.

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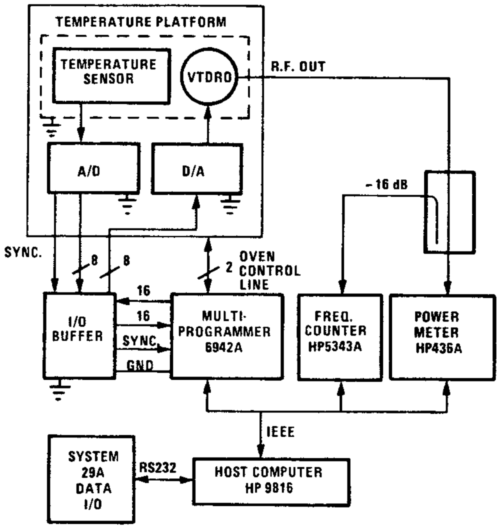

FIGURE 2. BLOCK DIAGRAM AUTOMATIC TEST SYSTEM

Figure 3 shows the frequency drift vs temperature for a digitally compensated FET DRO at 13.8 GHz. The uncompensated frequency drift characteristic is curve "a"; the compensating tuning voltage applied to the varactor is curve "b"' the theoretical frequency drift is curve "e"; the compensated DRO drift (cold to hot) is curve "d" and (hot to cold) is curve "c". The digitally stabilized DRO utilized an eight bit word which provides 256 break points for compensation. The total frequency drift is better than $\pm$20 ppm over the -55°C to +85°C temperature range.

ANALOG COMPENSATION

Many oscillator applications do not require such high frequency stability. For these applications, an analog compensator consisting of a temperature sensor and compensation circuit has been developed. Each oscillator is characterized by generating a tuning voltage vs temperature curve to maintain a constant frequency. The compensation circuit is aligned to fit the tuning voltage vs temperature curve of the oscillator. Consequently, the output of the circuit provides a correction voltage to the tuning varactor of the DRO thus maintaining a constant frequency over temperature.

The nonlinear correction voltage is produced by the analog circuit shown in Figure 4. Two break points are provided by the first stage. The break point voltages, V_{B1} and V_{B2}, and their respective slopes are controlled by select resistors R7, R4, R5, R15, R16 and R11. The second stage provides an offset aging adjustment which is independent of the breakpoint curve.

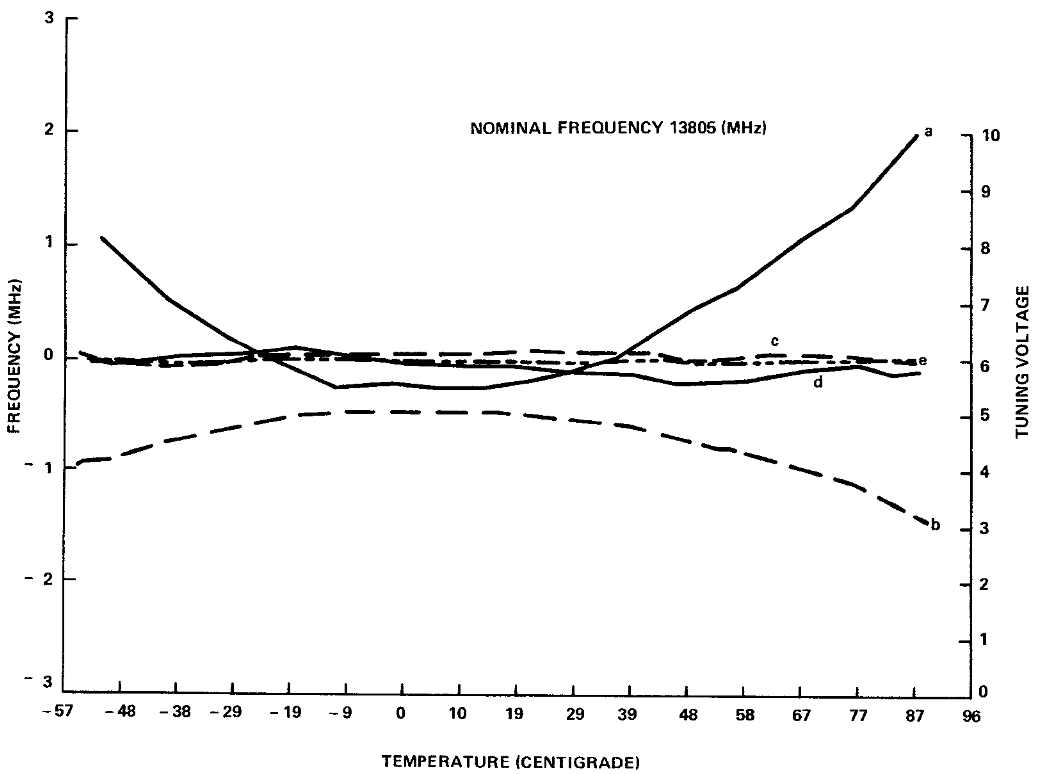

FIGURE 3. DIGITALLY COMPENSATED DRO FREQUENCY DRIFT AND TUNING VOLTAGE vs TEMPERATURE

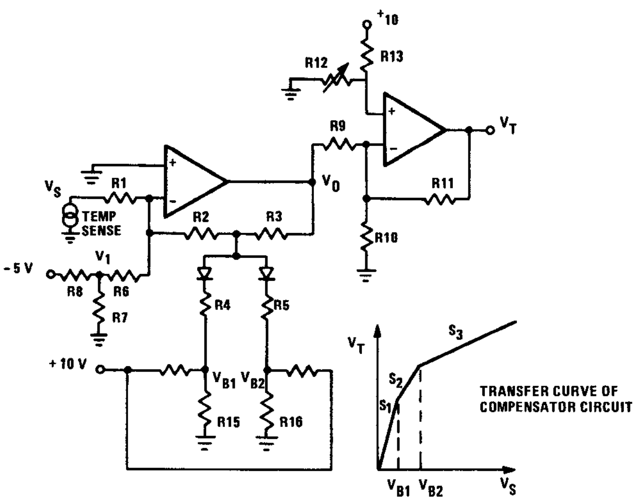

FIGURE 4. BREAKPOINT COMPENSATOR SCHEMATIC

Figure 5 shows an uncompensated frequency drift of 3 MHz for a FET DRO at 13.77 GHz, when measured from -55° to $+90^{\circ}C$. Analog compensation reduced the frequency drift to less than 500 kHz.

CONCLUSION

Digital and analog frequency - temperature compensation techniques have been developed which enable the dielectric resonator oscillator to achieve stability comparable to that of a crystal referenced oscillator over a military temperature range. No spurious signals are generated by these techniques.

REFERENCES

1. K. W. Lee and W. R. Day, "Varactor Tuned Dielectric Resonator GaAs FET Oscillator in X-band", 1982 IEEE MTT-S International Microwave Symposium Digest, pp. 274-276.

2. Daniel J. Dooley, "Data Conversion Integrated Circuits", 1980 IEEE press series.

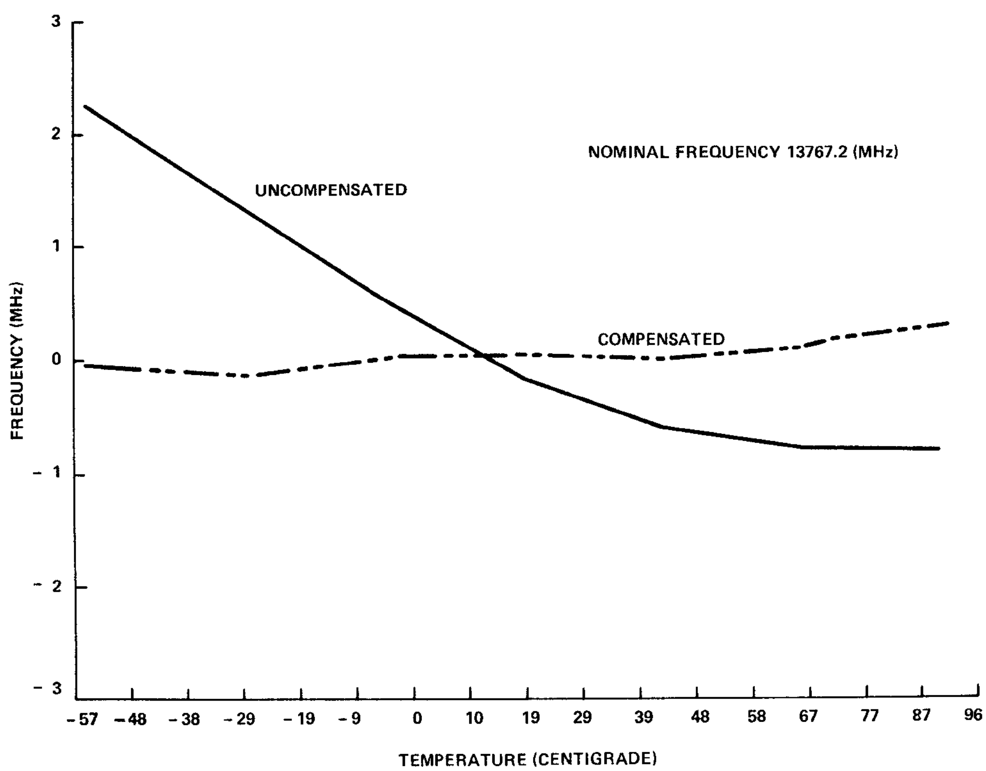

FIGURE 5. ANALOG COMPENSATED DRO FREQUENCY DRIFT vs TEMPERATURE